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DIGITAL CONTROL APPARATUS FOR A SWITCHING DC-DC CONVERTER

1. Field of the Invention

The present invention refers to a digital control apparatus for a switching DC-DC converter.

2. Background of the Invention

There is presently a continuous evolution of computers and above all of microprocessors. The need to process an always greater quantity of information in the shortest possible time has brought to manufacture high performance microprocessors that require high currents (which have a value of tens of amperes) for operation thereof. For this reason devices able to provide a low supply voltage and a high current have been manufactured.

However, the present microprocessors do not require high currents in continuous way but only in prefixed time periods; this is due to the quantity of operations that must be performed in said time periods. Therefore the value of the current adsorbed from them must change from tens of milliamperes to 80-100 amperes in a short time (a few nanoseconds).

Said devices are power supplies comprising switching DC-DC converters as, for example, the step-down converter shown in Figure 1. Said converter comprises a MOS power transistor M having a non-drivable terminal connected with an inductor L that in turn is connected with a real capacitor constituted by a capacitor Cr and a resistor R and which is placed in parallel with a load LOAD, for example a microprocessor. When the load LOAD has an abrupt variation, the average current that flows through the inductor cannot rise quickly to the value required by the load LOAD and the capacitor is discharged. The waveform of the output voltage Vout, which is shown in Figure 2a, will have a negative and positive voltage variation, respectively, at the start and at the end of the time period wherein a high current value is required by the load LOAD. If the variation of the current Iload (Figure 2b) on the load is given by ΔI, the instantaneous voltage variation will be, in first approximation, $\Delta V=\Delta I*R$.

The switching DC-DC converters are provided with control devices normally placed between the output and the driving terminal of the power transistor of said converters. The most utilized control devices are of the analog type but control devices of the digital type are presently being affirmed which present numerous advantages with respect to the analog control devices. In fact they are less sensitive to environmental variations, are less sensitive to noise, have less sensitivity to parameter variations and also the change of the control device does not require the change of its components. The last feature allows them to have a higher flexibility with respect to control devices of the analog type because it is not necessary to change the electric components of the control device for conforming to different circuit applications.

The digital control devices are provided with an analog/digital converter able to measure the output voltage and/or current of the DC-DC converter. The information deriving from the analog/digital converter is then processed by means of a digital control algorithm. The signal generated by the algorithm is sent to the input of a PWM device the output signal of which is used to drive the power transistor of the DC-DC converter.

However, the digital control devices have a main disadvantage due to the time delay in the control loop needed for processing the information. For this reason the digital control devices that are now present in commerce do not assure that the supply voltage of the load placed downstream of the DC-DC converter is kept constant without going down a voltage level that is equal to the minimum operation value of the load when the same load requires high currents.

A digital control device for a DC-DC converter is disclosed in the article "Modeling and Simulation of new digital control for power conversion systems" Capponi, G.; Livreri, P.; Minieri, M.; Marino, F. Power Electronics Specialists Conference, 2002, pesc 02. 2002 IEEE 33rd Annual, Volume 1, 2002 Pages: 155 – 158. In such article a technology of voltage positioning (VP) is used to minimize the excursion of the output voltage with the load variations. Figure 3 shows the waveform of the output voltage Vo and of the current Iload in the load LOAD of the generic converter in Figure 1 by using the control device that is present in said article: the voltage Vo shows peaks of the order of 400mV with load current variations of the order of 15 A.

SUMMARY

In view of the state of the art described, it is an object of the present invention to provide a digital control apparatus for a switching DC-DC converter that allows to lower further the excursion of the output voltage of the converter with the load variations.

According to present invention, such object is obtained by means of a digital control apparatus for a switching DC-DC converter, said converter comprising at least one power transistor and being able to provide a regulated output voltage on a load, said apparatus comprising control digital means having in input a reference digital signal and being able to provide a modulating signal to a PWM device, said PWM device having in input said modulating signal and providing an output square wave signal for driving the power transistor of said DC-DC converter, characterized by comprising digital means able to operate on the square wave signal to obtain that it has a non-linear modulation only when the value of a signal on the load is lower or higher than prefixed value range of said signal on the load.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and the advantages of the present invention will be made evident by the following detailed description of embodiments thereof, shown as not limiting examples in the annexed drawings, wherein:

Figure 1 is a circuit scheme of a DC-DC converter according to prior art;

Figures 2a and 2b show the voltage and the current in the load of the converter in Figure 1;

Figure 3 shows the diagrams of the voltage signal Vo and of the current signal Iload in an oscilloscope for the circuit in Figure 1 by using a digital control device according to prior art;

Figure 4a is a block scheme of a digital control apparatus for a DC-DC converter according to a first embodiment of the present invention;

Figure 4b is a block scheme of a digital control apparatus for a DC-DC converter according to a second embodiment of the present invention;

Figures 5a and 5b show the possible waveform of the output signal of the block PUSH of the device in Figures 4a or 4b;

Figures 6a-6c show time diagrams of the output signals of various circuit

blocks present in the scheme in Figure 4a;

Figure 7 shows the diagrams of the voltage signal Vout and of the current signal Iload in an oscilloscope for the DC-DC converter in Figure 4a; and

Figures 8-10 are block schemes of a digital control apparatus for a DC-DC converter according to variants of the first and the second embodiment of the present invention.

DETAILED DESCRIPTION

In Figure 4a a block scheme of a digital control apparatus for a DC-DC converter according to a first embodiment of the present invention is shown. A digital control block 1 receives an input reference voltage Vref, that is a constant digital signal, and provides an output voltage Vc. The digital control block 1 is preferably performed by means of a PID.

The signal Vc is sent in input to a digital/analog converter 2 providing the correspondent output analog signal. The last signal and a slope signal SR generated by a device GR are in input to an analog PWM device 3 able to provide a signal D to drive the power transistor M belonging to a DC-DC converter 4, for example the converter shown in Figure 1.

The output signal Vout of the converter 4 is sent in input to a analog/digital converter 6; the digital signal Voutd is sent to a block PUSH able to provide a digital signal Vs that is added to or subtracted from the signal Vc in order to carry out a non-linear modulation of the square wave signal D in output from the PWM device 3. The block PUSH is formed by a series of programmable registers and the signal Vs is of the step ramp type and its duration Dt and its amplitude A are programmable.

The signal Vs is emitted when the output voltage Vout goes under a lower threshold value or rises over a top threshold value, that is when said voltage Vout is out of a prefixed range of the output voltage Vout, for example if the voltage Vout is higher or lower than the 5% of its stationary value; more precisely the signal Vs is emitted during the transitions of the output voltage Vout or of the current Il flowing through the inductor L which are due to a variation of the load LOAD of the converter 4. Also the effect of such signal must not last for a long time, therefore it is necessary that said effect decreases in a gradual way. For these reasons the signal Vs has a

waveform as shown in Figures 5a or 5b.

Preferably the output voltage signal Voutd of the converter 6 is sent to an adaptive voltage positioning block (AVP) 5 having in input even a digital signal Vsensed, that is for example the signal Vsense deriving from a sense resistor Rs placed in series with the inductor L of the DC-DC converter which is made digital by the block 6. In the block 5 the digital signal Vsensed is multiplied by the value of the resistor Rs, divided by the value of the resistor R5, which has an equal or different value with respect to the value of the resistor R, and summed to the digital signal Voutd. The resulting signal is in output from the block 5 and is subtracted from the signal Vref and is sent to the block 1.

In Figure 6a the slope signal SR and an analog signal VM given by the sum or the difference between the modulating signal Vc and the signal Vs are shown. Said sum or difference are due to the positive or negative variations of the output voltage Vout; in fact if the variation of the load LOAD causes an elevation of the voltage Vout a signal Vs as shown in Figure 5b will be obtained; if instead the variation of the load LOAD causes a decrease of the voltage Vout a signal Vs as shown in Figure 5a will be obtained. The output signal D of the PWM block 3 is a non-linear modulated square wave signal (Figure 6b). Said signal D drives the power transistor M of the DC-DC converter by increasing or decreasing the on time Ton that is by modulating the duty-cycle. In such way the increase of the time Ton causes an increase of the current IL flowing through the inductor L (which is represented by a continuous tract with respect to the sketch tract) for satisfying the current requirement from the load LOAD while a decrease of the Ton time allows the inductor L to be easily discharged and to be quickly brought into the new stationary state.

In Figure 7 the oscilloscope measurements of the voltage signal Vout and of the current signal Iload for the circuit in Figure 4a are shown; it may be noted that the voltage Vout has a voltage drop of 150mV in correspondence of load current variations of the order of 15 A and it does not present the voltage peaks of the signal Vo in figure 3.

In Figure 4b a block scheme of a digital control apparatus for a DC-DC converter according to a second embodiment of the invention is shown. The control apparatus of said second embodiment is different from the control apparatus of the

first embodiment for the presence of a digital PWM device 9 instead of the analog PWM device 3. In such a way the digital/analog converter 2 does not occur and the signal to be modulated is of digital type and is generated inside the block 9.

Alternatively, according to variants of the above mentioned embodiments, the signal Vs may be sent in input to the control block 1 (Figure 9) instead that to the PWM device. According to other variants the block PUSH may be controlled by means of a signal present in the sense resistor Rs, that is the current IL or the voltage Vsense proportional to the current IL, which is always a signal proportional to the current variation of the load LOAD; the output signal Vs of the block PUSH may be sent in input to the PWM device (Figure 8) or to the control block 1 (Figure 10). The block PUSH comprises numeric comparators able to compare the output signal Voutd of the converter 6 with said prefixed voltage value range (block PUSH in Figures 4 and 9) or able to compare the voltage signal Vsensed proportional to the current signal IL or the current signal IL that has been digitalized respectively with a prefixed voltage value range or with a prefixed current value range (block PUSH in Figures 8 and 10), that is for example if the voltage Vsense or the current IL is higher or lower than the 5% of its stationary value. Even if in Figures 8-10 only apparatus as variants of the first embodiment of the present invention are shown, the features of the variants in Figures 8-10 are valid for the second embodiment of the present invention.

While there have been described above the principles of the present invention in conjunction with specific memory device layout and circuitry, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it

mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

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